AW-CMA02

IEEE 802.11 a/b/g/n/ac Wireless LAN
Bluetooth 5.2 Automotive Combo Module

Layout Guide

Rev. A

Revision History

Version	Revision Date	Description	Initials	Approved
A	2022/7/25	● Initial Version	YuFu Chen	

1. INTRODUCTION

This document provides key guidelines and recommendations to be followed when creating AW-CMA02 layout. It is strongly recommended that layout be reviewed by AzureWave engineering team before released for fabrication.

The following is a summary of the major items that are covered in detail in this application note. Each of these areas of the layout should be carefully reviewed against the provided recommendations before the PCB goes to fabrication.

- Ground Layout
- Power Layout
- Digital Interface
- RF Trace
- The other layout guide Information

2. Ground Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

(1) The top layer of customer platform should keep **complete ground plane as possible as you can, in order to be connected for all ground pins of AW-CMA02 module**.

(2) The area under our module forbidden any trace and via on top layer of customer platform.

3. Power Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

(1) Power traces shall surround ground to get stable and make sure all power traces have good return path to ground.

(2) Do not get close to digital traces (PCIe, UART) or continuous data traces, there could be coupling noise affect power traces and IC.

4. Digital Interface

Please follow power and ground layout guidelines. Here are some general rules for customers' reference.

(1) The digital Interface to the module must be well routed to minimize coupling to power planes and other digital signals.

(2) PCIe and UART traces need GND surrounded.

(3) PCIe & UART traces as possible away from CLOCK signal.

(4) The PCIe trace should be impedance controlled to 100 ohm.

5. RF Trace

The RF trace is the critical to route. Here are some general rules for customers' reference.

(1) The RF trace impedance should be 50Ω between ANT port and antenna matching network.

(2) The length of the RF trace should be minimized.

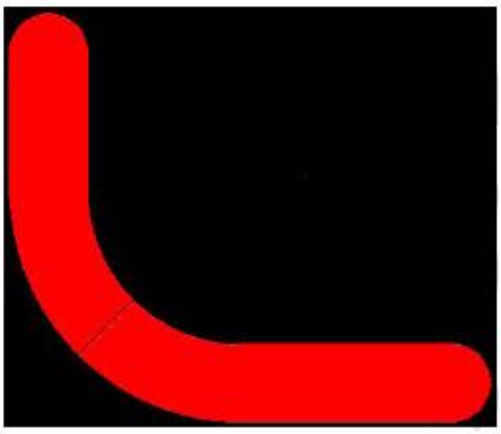
(3) To reduce the signal loss, RF trace should laid on the top of PCB and avoid any via on it.

(4) The CPW (coplanar waveguide) design and the microstrip line are both recommended; the customers can choose either one depending on the PCB stack of their products.

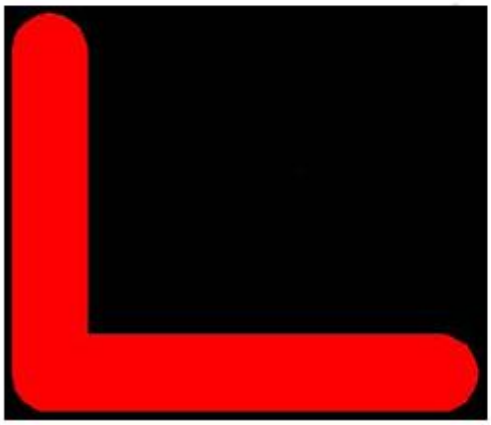
(5) The RF trace must be isolated with aground beneath it. Other signal traces should be isolated from the RF trace either by ground plane or ground vias to avoid coupling.

(6) To minimize the parasitic capacitance related to the corner of the RF trace, the right angle corner is not recommended.

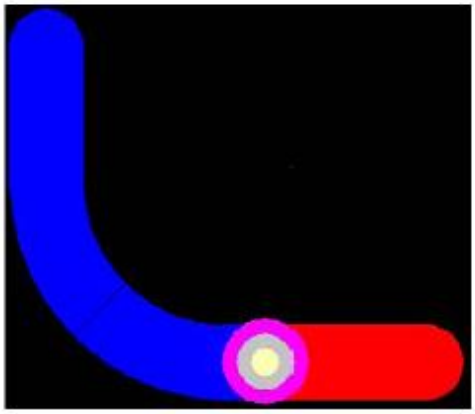
If the customers have any problem in calculation of trace impedance, please contact Azurewave.



Correct RF trace



Right-angled corner



Via on RF trace

Incorrect RF trace

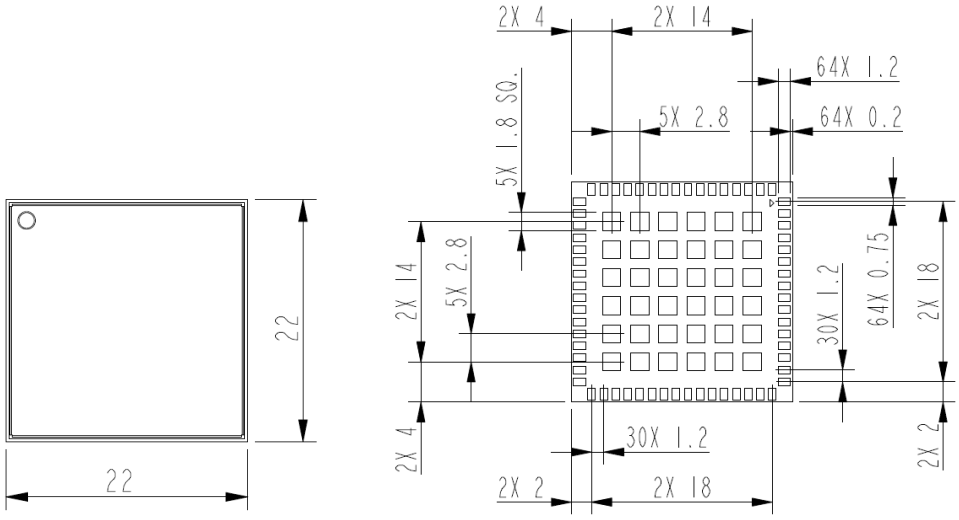
6. The other layout guide Information

1. Keep the module unused function pins floating.
2. Good power integrity of VDD will improve the signal integrity of digital interfaces.

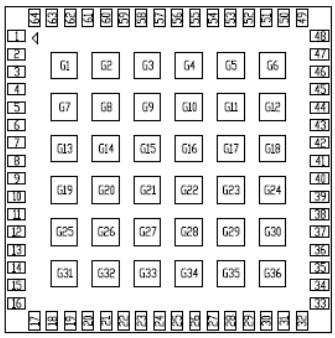
7. Footprint and stencil aperture recommendation

Footprint shares the same center with pin pad land, and follows below rule to define the size.

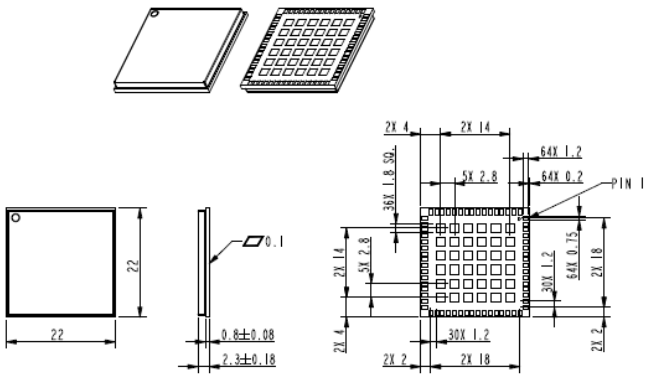
1. Rectangle type:
   1.1 Outermost layer :
   Footprint length = 1 * (pin pad land length)
   Footprint width = 1 * (pin pad land width)
   1.2 Others: the same size with pin pad.
2. Stencil aperture suggestion
   2.1 The pad size is same size with footprint.
3. Stencil thickness suggestion:
   3.1 Normal type product thickness: 0.1mm~0.12mm.
4. Solder printer opening and customer PCB footprint suggest.



8. Mechanical Drawing



PIN DEFINED (TOP VIEW)



TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm

			AzureWave				MODEL NO.		DESCRIPTION					DOCUMENT LEVEL	
									OUTLINE DRAWING					CONFIDENTIAL	
			DIM.	X≤80	80<X≤180	180<X≤315	315<X≤800	PART NO.	DRAWING NO.	MATERIAL	UNIT	SCALE	REV	PAGE	DATE	DESIGNED
ITEM	DESCRIPTION	DATE	TOL.	±0.1	±0.15	±0.20	±0.25		R2-2A02-CDD-01		mm	2/1	A	1/1	2022/07/01	STEVE CHANG